IN THE SPECIFICATION

Please make the paragraph substitutions indicated below. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

#18 1-7-04

The paragraph beginning on page 1, line 4 is amended as follows:

The inventive subject matter ~~present invention~~ is directed to shunting arrangements to reduce high currents in grid array connectors.

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The paragraph beginning on page 1, line 8 is amended as follows:

Background and example embodiments of the inventive subject matter ~~present invention~~ may be described using the context of processors and semiconductor package grid array mounting arrangements, but it is submitted that practice of the inventive subject matter ~~present invention~~ and a scope of the appended claims are not limited thereto.

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The paragraph beginning on page 2, line 5 is amended as follows:

The foregoing and a better understanding of the inventive subject matter ~~present invention~~ will become apparent from the following detailed description of example embodiments and the claims when read in connection with the accompanying drawings, all forming a part of the disclosure of this inventive subject matter ~~invention~~. While the foregoing and following written and illustrated disclosure focuses on disclosing example embodiments of the inventive subject matter ~~invention~~, it should be clearly understood that the same is by way of illustration and example only and that embodiments of the invention are [[is]] not limited thereto. Such embodiments of the inventive subject matter may be referred to, individually and/or collectively, herein by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. The spirit and scope of embodiments of the present invention are limited only by the terms of the appended claims.

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The paragraph beginning on page 3, line 16 is amended as follows:

Before beginning a detailed description of the inventive subject matter ~~invention~~, mention of the following is in order. When appropriate, like reference numerals and characters may be used to designate identical, corresponding or similar components in differing figure drawings. Further, in the detailed description to follow, example sizes/models/values/ranges may be given, although embodiments of the present invention are [[is]] not limited to the same. Example arbitrary axes (e.g., X-axis, Y-axis and/or Z-axis) and/or example arbitrary column (C) and row (R) directions may be discussed/illustrated, although practice of embodiments of the present invention is not limited thereto (e.g., differing axes/column/row directions may be able to be assigned). Well-known power/ground connections to ICs and other components may not be shown within the FIGs. for simplicity of illustration and discussion, and so as not to obscure the inventive subject matter ~~invention~~. Further, arrangements may be shown in block diagram form in order to further avoid obscuring the inventive subject matter ~~invention~~, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the inventive subject matter ~~present invention~~ is to be implemented, i.e., such specifics should be well within purview of one skilled in the art. Where specific details (e.g., structures, circuits, flowcharts) are set forth in order to describe example embodiments of the invention, it should be apparent to one skilled in the art that the inventive subject matter ~~invention~~ can be practiced without, or with variation of, these specific details.

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The paragraph beginning on page 4, line 8 is amended as follows:

At this point, it is again stressed that the context of the example embodiments described ahead does [[do]] not limit practice of the inventive subject matter ~~present invention~~ or a scope of the appended claims. For example, although example embodiments of the present invention will be described using an example semiconductor package making use of a pin/socket mounting arrangement, practice of the inventive subject matter ~~invention~~ is not limited thereto, i.e., the inventive subject matter ~~invention~~ may be able to be practiced with other types of mounting arrangements (e.g., BGA, μBGA). Further, practice may be applicable to non-package arrangements, e.g., to mount a pinned printed circuit board (PCB) such as an interposer board to

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another receiving substrate. That is, the term "receiving substrate" may be generically used to describe the component (e.g., motherboard) upon which the first component, i.e., an "interfacing substrate" (e.g., semiconductor package, interposer board, PCB) is mounted. Finally, while example embodiments of the present invention will be described using an example semiconductor processor in a computing system environment, practice of the inventive subject matter ~~invention~~ is not limited thereto, i.e., the inventive subject matter ~~invention~~ may be able to be practiced with other types of systems, and in other types of environments (e.g., chip sets, graphics chips, and automotive, military and flight communication systems).

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The paragraph beginning on page 4, line 23 is amended as follows:

Turning now to a detailed description, FIG. 1 illustrates a side view 100 of a semiconductor package 110 mounted via pins or connectors onto a mounting assembly or socket assembly 120 electrically connected (e.g., soldered) to a receiving substrate 130 such as a PCB (e.g., motherboard), such view being useful in explanation and understanding of background and example embodiments of the present invention. The semiconductor package 110 may contain an example processor die 140 and at least one interfacing substrate 150 (e.g., a chip carrier PCB), and typically additionally includes an optional interposer PCB (not shown). The die 140 may be mounted and electrically connected to the interfacing substrate 150 using, for example, a grid array of electrically conductive bumps/balls 145 and a corresponding array of pads/vias 157.

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The paragraph beginning on page 8, line 21 is amended as follows:

The receiving substrate 130 and the semiconductor package 110 may have conductive patterns in the form of power and ground plane, pad, and via locations compatible with the shunt(s). By moving the transfer of large currents from the grid array pin/socket pairs, the occurrence of excess power conduction through the pin/socket pairs is drastically decreased. Use of the shunting embodiments is expected to remove the previously discussed reliability concerns that involve heat, and is expected to lessen a size and weight of any implemented heat spreader or heat sink. The shunting embodiments of the present invention are able to handle anticipated extremely high current needs of future electrical devices.

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The paragraph beginning on page 9, line 4 is amended as follows:

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FIG. 4 is similar to FIG. 2, but shows a top view 400 of the FIG. 3 example locations of the shunt embodiments inside the reserved component area. The shunts may individually serve a grounding, or power transfer, function. The FIGS. 3-4 example embodiment may result in little impact to the existing pin and socket layout, as the shunts are wholly provided within the reserved component area 160.

The paragraph beginning on page 9, line 9 is amended as follows:

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FIG. 5 is a perspective see-through view 500 illustrating example contact footprints of the example FIG. 4 shunt embodiment relative to a receiving substrate's layering arrangement. Such electrical planes 135 may be power planes 510 (including power pads 530 and power vias 535), or ground planes 520 (including ground pads 540 and ground vias 545) for transfer of power currents. FIG. 5 also illustrates example contact footprint locations of the shunts 310', 310" onto the power pads 530 and ground pads 540. Potential electrical contact areas between any shunt 310 (FIG. 3) and a conduction path of the interfacing substrate 150, of the receiving substrate 130, and of the socket assembly 120, are referred to herein as a "conductive pattern" and may include, but are not necessarily limited to, a power plane 510 (FIG. 5), a power pad 530, a power via 535, a ground plane 520, a ground pad 540, and a ground via 545. Thus, a shunt 310 (FIG. 3) may be electrically coupled between any of the foregoing types of conductive patterns of an interfacing substrate, of a receiving substrate, and/or of a socket assembly.

The paragraph beginning on page 9, line 15 is amended as follows:

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The respective pads may in turn electrically connect to the power and ground planes of the receiving substrate through the vias. Maximizing the number of vias under each respective power pad 530 or ground pad 540 may aid in lowering the resistance from the receiving substrate electrical planes 135 to the shunt. Such a low resistance DC shunt path helps reduce a maximum current which may flow in any original pin/socket pair which remains connected in parallel with the lower resistance shunt (i.e., the current will prefer the low resistance path). Proper layout and

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design of shunts ~~shunt~~, vias and the low resistance path may also be used to control and/or increase a uniformity of current flow within one or both of the receiving substrate (e.g., motherboard) and the interfacing substrate (e.g., package, interposer).

The paragraph beginning on page 10, line 19 is amended as follows:

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FIG. 8 is a top view 800 illustrating the FIG. 7 example shunt locations, with the shunts 310 passing through openings in an area 810 outside of pin and socket array area, or passing through an area 820 inside of the pin and socket contacts array area. To accommodate these locations, appropriate modifications may be needed to the receiving substrate, interfacing substrate and/or socket assembly. Again, care must be taken such that each shunt does not obstruct, is not in direct contact with, or in arcing distance to, any pin/socket pair or any other component.

The paragraph beginning on page 13, line 7 is amended as follows:

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This concludes the description of the example embodiments. Although the inventive subject matter ~~present invention~~ has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this inventive subject matter ~~invention~~. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the inventive subject matter ~~invention~~. In addition to variations and modifications in the component parts and/or arrangements, alternative uses also will be apparent to those skilled in the art.

The paragraph beginning on page 13, line 16 is amended as follows:

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For example, with regard to semiconductor packages, practice of the inventive subject matter ~~invention~~ is not limited to the above-mentioned pin array, and a non-exhaustive listing of other packages may include a bump/ball grid array. With regard to mechanical connection, the

practice of the inventive subject matter ~~invention~~ is not limited to the FIGs. 11 and 12 connections, and any other fastener object/feature may likewise be provided. For example, a non-exhaustive listing may include welding and glue (e.g., conductive glue). With regard to reduced electrical resistance, a non-exhaustive listing of an alternative approach may include using a shunt material of lower resistance material than a pin/socket material. In addition, the inventive subject matter ~~invention~~ is not limited to implementation with processor packages, and instead, may be used for shunting in other electrical components.

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